

**APPLICATION  
FOR  
UNITED STATES LETTERS PATENT**

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**TITLE:** SEMICONDUCTOR DEVICE AND  
METHOD HAVING MULTIPLE  
SUBCOLLECTORS FORMED ON  
A COMMON WAFER

**DOCKET NO.:** BUR920000140US1

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# SEMICONDUCTOR DEVICE AND METHOD HAVING MULTIPLE SUBCOLLECTORS FORMED ON A COMMON WAFER

## DESCRIPTION

### FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a method of fabricating a chip with bipolar transistors having different optimum unity current gain cutoff frequency ( $f_T$ ) and/or breakdown voltage (BVCEO and BVCBO).

### BACKGROUND OF THE INVENTION

Currently, bipolar transistors are utilized in a myriad of high frequency communications applications. Many bipolar transistors feature a buried subcollector to assist in the collection of carriers while reducing series resistance. *series collector very thin* See e.g. U.S. Patent 5,286,997, "METHOD FOR FORMING AN ISOLATED, LOW RESISTANCE EPITAXIAL SUBCOLLECTOR FOR BIPOLAR TRANSISTORS," issued February 15, 1994 to Hill and assigned to Texas Instruments.

More recently, higher switching speeds have been achieved by utilizing heterojunction bipolar transistors (HBT's), in which bipolar transistor elements are formed in graded SiGe or SiGeC layers that enhance carrier mobility. See e.g. U.S. Patent 5,633,179, "METHOD OF FORMING SILICON/SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTOR," issued May 27, 1997 to Kamins et al. See e.g. U.S. Patent 5,506,427, "HETEROJUNCTION BIPOLAR TRANSISTOR WITH SILICON-GERMANIUM BASE," issued April 9, 1996 to Imai and assigned to NEC Corporation.

Another alternative that has developed is BiCMOS, which attempts to combine the high frequency operations of bipolars with the low power attributes of CMOS. See e.g. U.S. Patent No. 5,856,695, "BICMOS DEVICES," issued January 5, 1999 to Ito et

al., and assigned to Harris Corporation.

## SUMMARY OF THE INVENTION

The inventors have discerned situations in which it would be advantageous to vary the optimum unity current gain cutoff frequency ( $f_T$ ) and/or breakdown voltage (BVCEO and BVCBO) for bipolar transistors on a common wafer. Since according to the Johnson limit the relationship between  $f_T$  and BVCBO are interrelated, the semiconductor devices resulting from the present invention may be designed to take full advantage of the interrelationship.

In a first aspect, the present invention is a semiconductor wafer comprising a first device having a first subcollector; and a second device having a second subcollector, wherein the second subcollector differs from said first subcollector.

In a second aspect, the present invention is a first and second bipolar transistors formed on a p-substrate, said first transistor comprising a Sb subcollector; a n-epi collector; a SiGe polysilicon p-doped extrinsic base; a SiGe silicon single crystal intrinsic base; and said second transistor comprising: an As subcollector; a n-epi collector; a SiGe polysilicon extrinsic base; and a SiGe Si single crystal extrinsic base.

In a third aspect, the present invention is a method of manufacturing a semiconductor device on a wafer comprising the steps of forming a subcollector region by implantation of the wafer with a first dopant and with a second dopant; forming an isolation structure on the subcollector region; forming a SiGe film or SiGeC film on the wafer surface for formation of a transistor base region; forming an emitter structure on the SiGe or SiGeC film.

Still other objects and advantages of the present invention will become readily apparent by those skilled in the art from the following detailed description, wherein it is shown and described only the preferred embodiments of the invention, simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from

the invention. Accordingly, the description to be regarded as illustrative in nature and not as restrictive.

## BRIEF DESCRIPTIONS OF THE DRAWINGS

The above-mentioned objects and advantages of the present invention will be more clearly understood when considered in conjunction with the accompanying drawings, in which:

FIGS. 1-16 are schematic diagrams showing a segmented view of a device illustrating in different steps of the fabrication process one embodiment of the present invention.

FIGS. 17-20 are schematic diagrams illustrating a device in different steps of the fabrication process of another embodiment of the present invention.

FIG. 21 is a diagram of a further embodiment of the present invention which shows a cross section of an epitaxial graded Germanium-base Silicon Germanium (SiGe) heterojunction bipolar (HBT) device with a polysilicon deep trench isolation.

FIG. 22 shows the base-collector ESD robustness of SiGe HBT for different epitaxial Arsenic (As) subcollector doses.

FIG. 23 shows the ESD robustness of a SiGe HBT for epitaxial Arsenic (As) and Sb subcollectors.

FIG. 24 shows the ESD results of an Sb SiGe varactor structure versus an Arsenic (As) SiGe varactor for a positive HBM pulse.

FIG. 25 shows the ESD results of an Sb SiGe varactor structure versus an Arsenic (As) SiGe varactor for a negative HBM pulse.

## DESCRIPTION OF PREFERRED EMBODIMENTS

In order to facilitate an understanding of the different embodiments of the present invention, reference will be made to the figures which illustrate a diagrammatic representation of the steps of the different embodiments of the present invention.

Figures 1-16 show the process steps for manufacturing one embodiment of a semiconductor device of the present invention.

Radio frequency products need enhanced ESD protection to achieve a good  $f_T$  and  $f_{MAX}$  device characteristics. The present invention provides a device and manufacturing method for providing multiple npn SiGe transistors, varactors, and Schottky diode structures with different subcollectors for functional and ESD advantages for SiGe technology.

For RF products there is also a need to provide devices having high breakdown voltages, ESD robust elements and low capacitance. The inventors have found that semiconductor process doping concentrations and design dimensions can have a significant influence on the high pulse current and ESD sensitivities of SiGe semiconductor devices. More specifically, the inventors have found that by controlling collector lateral ballasting ESD linearity may be improved.

According to one embodiment of the present invention, a semiconductor wafer 10 is provided. The semiconductor wafer 10, is typically silicon, for instance a P- type single crystal silicon substrate, but can be any semiconductor material. Figure 1 shows a P- substrate 12 upon which a photoresist layer 14 is formed. A portion of the resist layer 14 is removed forming a region 16 that exposes the P- substrate 10. A first dopant Arsenic (As) is implanted forming an N+ first subcollector region 18. Figure 2 shows that a second dopant Antimony (Sb) is then implanted into the first subcollector region 18.

Figure 3 shows the results of an N-epitaxial silicon growth step which includes an N- layer 20 formed over the P- substrate 12 and the N+ first subcollector region 18. Note that this epitaxial silicon is not required for the invention. A mask including a resist layer

22 is then formed over the N- layer 20 as shown in Figure 4. Two deep trenches 24, 26 may then be etched adjacent the boundaries of the N+ subcollector 18 in the resist layer 22 using RIE methods that remove silicon. Arsenic is then implanted with the resist 22 still in place to form channel stop regions 28, 30 at the bottom of each trench. Note these channel stops are not shown in subsequent figures for ease of illustration. The substrate is then oxidized to form oxide layers 32, 34 on the sidewalls of trenches 24, 26. The structure is subjected to brief blanket RIE to remove oxide from the bottom of the trenches as well as the upper surface of the substrate. Then a blanket layer of polysilicon is deposited to fill the trenches with poly 36, 38 as shown in Figure 5, and the polysilicon above the trenches is removed using well known chemical-mechanical planarization techniques.

Figure 5 shows a mask including a resist layer 40 (including a pad nitride layer 41) is then formed over the semiconductor wafer 10. The exposed portions of the wafer 10 are then etched to form silicon islands 42 above the N+ first subcollector region 18. Figure 6 shows the semiconductor wafer 10 after the trench planarization.

The next step is for the deep pedestal implant. Figure 7 shows that FET protective oxide layer 102 is deposited on the semiconductor wafer 10, followed by the deposition of a polysilicon protection layer 104 and oxide layers 106. A mask is then provided including a resist layer 108. The resist layer 108, oxide layers 106, polysilicon protective layer 104, and protective oxide layer 102 may then be etched and patterned forming a region 110 within the resist layer 108. The next step is the implant of a deep pedestal 112 into the region 110. The nitride strip 56 may then be etched. The next step is to remove the resist layer.

SM AB The emitter and extrinsic base is then defined. The next step is to deposit an LTE polysilicon layer 114 (e.g., NPN SiGe EPI base film) followed by the deposition of oxide and silicon layers 116, 118, 120, 122. This is followed by the step of growing and depositing of the emitter film layers 124, 126. Figure 8 shows the semiconductor wafer 10 after the LTE EPI and base film deposition.

A mask including a resist layer 128 is then provided on the semiconductor wafer 10 as shown in Figure 9. The resist layer 128 is then etched and patterned to define an

emitter region 130 and extrinsic base region. The spacer is then deposited and etched to therein define an emitter-extrinsic base spacing the emitter region 130. The next step is the extrinsic base implant as shown in Figure 10 to form the P+ region 131 and the P+ polysilicon layer 133.

Sub 134  
The emitter formation is then defined. Figure 11 shows the results of the etching of the emitter opening 132. The emitter window etch is followed by a mask which includes a resist layer 134 as shown in Figure 12. The resist layer 134 is then etched and patterned to provide an emitter window etch region 136 above the emitter opening 132. The next step is the pedestal 2 implant into the emitter opening 132. This step includes an emitter polysilicon layer deposit and the implant. The resist layer 134 is then removed followed by providing an N+ emitter polysilicon layer 138 and the deposit of emitter films 140.

FIG. 11  
The emitter formation of the polysilicon stack is continued. A mask including a resist layer 142 is then provided (Figure 13). The resist layer 142 may then be etched and patterned including the step of the NPN emitter polysilicon layer 138 and the etch of the emitter films 140. The remaining resist layer 142 may then be removed. Figure 13 shows that a mask including a resist layer 142 may then be provided on the semiconductor wafer 10. The mask is followed by the etching of the NPN emitter polysilicon layer 138 and emitter films 140.

The NPN base region is then defined. Figure 14 shows that a mask is then provided including a resist layer 144. The mask may be utilized to etch the NPN base polysilicon layer 133 and the protective oxide layer.

Sub 15  
A salicide block mask is then applied. Figure 15 shows that a mask may then be provided including a resist layer 152. The mask may be etched and patterned to form an NPN spacer and a resistor TiSix block. The patterning of the resist layer 152 is provided over the PCP resistor and N+ resistor region after etching resulting in the formation of an NPN spacer and a resistor space TiSix block and a titanium silicide. Titanium salicide is then formed. Figure 16 shows the semiconductor wafer 10 after the TiSix formation and the removal of the resist layer 152.

Successive metal steps are then established. The semiconductor wafer 10 may include two to five levels of metal (M2 to M5) including vias (V1 to V4). The next to last metal level (MT) may include a metal-to-metal capacitor. The semiconductor wafer will also include a thick last metal layer (AM) and a last via (LV). Alternative processes such as damascene copper can also be used for interconnects.

A final mask may be provided including an polyimide layer 168. The mask may be deposited, cured, patterned and etched before the final passivation step. The resulting structure is one in embodiment of the present invention.

According to another embodiment of the present invention, Figures 17-20 show the process steps to for manufacturing of a semiconductor device having subcollectors for first and second transistors. As shown in Figure 19 a semiconductor device 200 may include a substrate wafer 202 upon which a photoresist mask 204 is provided to define a first subcollector region 206 for a first transistor. The first subcollector region 206 is implanted with a dopant, for example, Arsenic (As), to therein form a first subcollector 208.

As shown in Figure 18, a second photoresist layer 204' may then be provided that defines a second subcollector region 210 for a second transistor. The second subcollector region 210 may be implanted with a dopant, for example, Antimony (Sb), to therein form a second subcollector 212. Alternately, the first subcollector 206 may be exposed to resist 204', so that region 206 receives by As and Sb while region 210 receives only Sb.

As such, first and second subcollectors 206, 212 differ in impurity type or combinations of impurity type, so that one transistor has a higher resistance and a higher collector base breakdown voltage than the other.

The next step is to remove the photoresist layer 204' as shown in Figure 19. The removal of the photoresist layer 204' may be followed by an epitaxial growth step by forming an epitaxy on the first and second subcollectors 206, 212 including layer 214 as shown in Figure 20. However, the step of epitaxial growth is not required.

An isolation structure (not shown) is then formed using conventional techniques on at least one subcollector region 208, 212. A SiGe or SiGeC film is then formed using conventional techniques on the wafer surface for formation of a transistor base region.



Finally, an emitter structure is then formed on the SiGe or SiGeC film.

Alternately, the subcollector doses may differ in doping concentration. To provide the desired differentials in performance, the levels of the doping concentrations should differ by at least one order of magnitude. For example, in one embodiment of the present invention, the As dose for subcollector 208 is on the  $1 \times 10^{16} \text{cm}^{-2}$  range, and second subcollector 212 may be implanted with As at a dose in the  $1 \times 10^{15} \text{cm}^{-2}$  range.

The features of the invention were more thoroughly explored by carrying out a series of experiments on the HBT shown in Figure 21. Note, for ease of illustration a single device is shown; in practice, the experimental chip was fabricated in accordance with the teachings of the invention, so that it had HBTs with differing subcollectors (in this case differing in dopant concentrations). More specifically, using UHV/CVD processing, SiGe was deposited in the base region over single-crystal silicon and shallow trench isolation (STI) structure. The Ge concentration was varied during the film deposition process for profile and device optimization of the SiGe HBT base region. The epitaxial region formed a single-crystal SiGe intrinsic base and an amorphous poly-SiGe extrinsic base region. A window was formed over the single crystal intrinsic SiGe base region to form the n-type polysilicon emitter. Interconnection to the emitter, base and collector was defined by a tungsten (W) local interconnect. Interlevel dielectrics, tungsten contacts, and aluminum interconnects were formed with the reactive ion etching (RIE) and chemical mechanical polishing (CMP) processes used in conventional CMOS technologies.

Experiments were performed on the structure shown in Figure 21 to explore the effect of subcollector doping concentration on SiGe HBT device human body model (HBM) ESD robustness, and the linearization with structure size due to a subcollector lateral resistor ballasting effect at high subcollector sheet resistances. By "ballasting," we refer to the operation of the subcollector in inhibiting the lateral redistribution of current. The lateral subcollector ballasting effect was demonstrated by both doping concentration and dopant type. The experimental results show the effects and role of the subcollector in high current applications and ESD events. In addition, the experimental results show a small impact on the optimum unity current gain cutoff frequency ( $f_T$ ) and the unity power

gain cutoff frequency  $f_{\text{MAX}}$ . The experimental results also show the tradeoff between  $f_T$ ,  $f_{\text{MAX}}$ , and ESD for an SiGe device. For example, Figure 22 shows the base-collector ESD robustness of SiGe HBT for different epitaxial subcollector doses. For example, Figure 40 shows the ESD robustness of a SiGe HBT for epitaxial As and Sb subcollectors.

Figure 22 illustrates the ESD results in a base-collector configuration of a SiGe HBT 0.32  $\mu\text{m}$  emitter width as a function of the emitter length, where the subcollector is As-doped at varying concentrations. The experimental results show that the ESD results improve as a function of emitter length, though not linearly. However, as the doping concentration of the subcollector decreases, ESD robustness improves with emitter length in a more linear fashion. This is because the higher sheet resistance provides lateral subcollector ballasting within the subcollector region. At high current, non-uniform self heating along the current structure leads to current redistribution along the length of the structure. The experiments show that higher sheet resistance subcollectors inhibit the lateral redistribution of the current. This leads to a linear scaling with the size of the transistor structure.

Figure 23 shows the results of a second study using Sb as the subcollector which shows this same effect and net improvement. With a 80  $\Omega/\text{square}$  subcollector, ESD results were superior to the 8  $\Omega/\text{square}$  subcollector (e.g.,  $1 \times 10^{16}/\text{cm}^2$ ) and showed improved ESD linearity. One reason for the improvement is postulated to be related to the fact that the high doped region of the Sb subcollector is farther away from the base-collector junction preventing diode shorting as well as the reason that the dopants Sb do not diffuse as far as arsenic for a given self heating temperature. Additionally it is postulated that the volumetric region which is undergoing self-heating is physically larger. Another physical reason is that the subcollector has more natural resistive ballasting laterally along the length of the collector providing a better scaling with varactor length.

Figure 24 shows the ESD results of an Sb SiGe varactor structure versus an As SiGe varactor for a positive HBM pulse. For negative pulses it is noted that the Sb subcollector ESD results are superior to the As subcollector in its magnitude and scaling

dependence. The Sb subcollector breakdown voltages are at least three times better than the As subcollector which is important for RF applications when this structure is used in a forward or reverse configuration for ESD devices. Figure 25 shows the ESD results of an Sb SiGe varactor structure versus an As SiGe varactor for a negative HBM pulse.

In the invention, the varying subcollectors may be part of a transistor, bipolar transistor, a Schottky barrier diode, a PIN diode, a p<sup>+</sup>/subcollector diode, a p<sup>+</sup>/n-well/subcollector diode, a pn diode or a varactor. Moreover, in the invention an additional diffusion may optionally be included abutting the first subcollector and/or second subcollector. The additional diffusion may include a "pedestal" implant (i.e. an implant that abuts the subcollector and is formed by implantation through the emitter window in the collector region) and/or a reachthrough diffusion. The first subcollector and/or second subcollector may also have an edge defined by a step (e.g. by an STI region).

In the present invention, a first bipolar transistor comprising a first subcollector and a second bipolar transistor comprising a second subcollector are formed on a common substrate. The second subcollector differs from the first subcollector in impurity type and/or doping concentration, and/or in any other fashion that results in a marked differential in sheet resistance. For example, the first subcollector may comprise an implant dose in the  $1 \times 10^{16} \text{cm}^{-2}$  range and the second subcollector may comprise an implant dose in the  $1 \times 10^{15} \text{cm}^{-2}$  range. Sheet resistance of the  $1 \times 10^{16} \text{cm}^{-2}$  dose is typically 10  $\Omega/\text{square}$  whereas  $1 \times 10^{15} \text{cm}^{-2}$  is near 100  $\Omega/\text{square}$ . As such, the second subcollector provides a higher resistance and a higher collector base breakdown voltage than the first subcollector. As a practical matter, this resistance differential can be increased by reducing the concentration of the second subcollector still further - e.g. to  $1 \times 10^{14} \text{cm}^{-2}$  and below. However, the best tradeoff between introducing a sufficient differential in resistance without reducing overall transistor performance appears to be keeping the first subcollector at a resistivity of about 5-20  $\Omega/\text{square}$ , and the second at 50-200  $\Omega/\text{square}$ , respectively.

The invention may be applied to various integrated circuit structures and substrates. For example, the invention may be applied to epitaxial or non-epitaxial

Sub  
AZ  
Cont

substrate, or to HBTs with Si, SiGe, or SiGeC bases. The base region may comprise a "raised base device". The emitter may be a self-aligned emitter, non-self aligned emitter, or a quasi-self aligned emitter. The higher sheet resistance subcollectors may be applied to devices utilized to provide thermal stability, ESD protection, or a high-power device operations for improved power-to-failure. In particular, ESD protection may be provided by high sheet resistance subcollectors in diodes, varactors, or Schottky elements.

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In still a further embodiment according to the present invention, a semiconductor structure may comprise a first transistor comprising a p-substrate, an As subcollector, an n-epi collector, a SiGe polysilicon p-doped extrinsic base, and a SiGe silicon single crystal intrinsic base; and a second transistor comprising a p-substrate, an Sb subcollector, a n-epi collector, an SiGe polysilicon p-doped extrinsic base, an SiGe silicon single crystal intrinsic base; where the first and said second transistors exist on the same substrate and where said second structure is used for ESD protection.

The present invention also provides a means of providing a subcollector region of a transistor of a dopant end type which has low diffusivity to avoid dopant diffusion of the implants during self heating events.

The present invention can be practiced by formation of implanted subcollectors without epitaxial growth. Hence an implanted subcollector can be formed using an Arsenic subcollector implant step and an Antimony subcollector implant step. This is followed by activation steps to activate the dopants. These and other modifications to the foregoing teachings may be made by persons of skill in the art without departing from the spirit and scope of the present invention as set forth in the accompanying claims.

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